

NMUX1308-Q100

1.5 V to 5.5 V, 8-channel analog switch multiplexer and demultiplexer with injection-current control

Rev. 1.4 — 23 August 2024

Product data sheet

1. General description

The NMUX1308-Q100 is a general purpose, CMOS, bi-directional, 8 channel analog switch, with an operating voltage range of 1.5 V to 5.5 V. The NMUX1308-Q100 is dual source compatible with existing 4851 and 4051 devices. The NMUX1308-Q100 extends the digital logic thresholds to be compatible with 1.8 V systems without the need for voltage translation.

The analog signal pins are comprised of a common input/output (Z) and eight independent inputs/outputs (Y0 to Y7). All analog signal pins are bi-directional and support a voltage range from GND to V_{CC} .

All analog signal pins integrate injection current control circuitry. This control circuitry isolates overvoltage spikes on disconnected analog signal pins from coupling to the connected analog signal path, thereby preserving measurement accuracy. Additionally, this integration makes the use of external overvoltage clamp components (e.g. resistive diode network) unnecessary.

There are four control signal pins (S0, S1, S2, and \bar{E}). S0, S1, and S2 determine the analog channels to connect between Z and Yn. \bar{E} can be used to override S0, S1, and S2, disconnecting all analog channels.

The control signal pins support 1.8 V logic thresholds across all operating voltages. In addition, these pins are 5.5 V tolerant, enabling up to 5.5 V operation independent of supply voltage.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- SP8T-Z functionality
- Wide operating range: 1.5 V to 5.5 V
- Rail-to-Rail operation on analog signal pins
- Injection current control
- 1.8 V digital logic thresholds
 - Digital pins compatible with 1.8 V logic thresholds across full V_{CC} range
 - Removes need for up-translation device for compatibility with low voltage GPIOs
- I_{off} circuitry
 - Enables wider latitude for power sequencing considerations
 - Isolates backflow between supply rail and any biased digital/analog input when $V_{CC} = 0$ V
 - Prevents any biased digital/analog input from backpowering V_{CC} when $V_{CC} = 0$ V
 - Maintains Hi-Z state of analog switch when $V_{CC} = 0$ V
- 5.5 V overvoltage tolerant digital inputs
 - Supports switching of 5.5 V digital signals across full V_{CC} operating range
 - Removes need for down-translation when switching thresholds are met
- Pin compatible with industry standard 4051 and 4851 analog switch products
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C2b exceeds 750 V
- DHVQFN package with Side-Wettable Flanks enabling Automated Optical Inspection (AOI) of solder joints

1.5 V to 5.5 V, 8-channel analog switch multiplexer and demultiplexer with injection-current control

3. Applications

- Body control module
- Battery management system
- Automotive head unit

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NMUX1308PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
NMUX1308BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Marking

Table 2. Marking

Type number	Marking code
NMUX1308PW-Q100	NMU1308
NMUX1308BQ-Q100	NM1308

6. Functional diagram

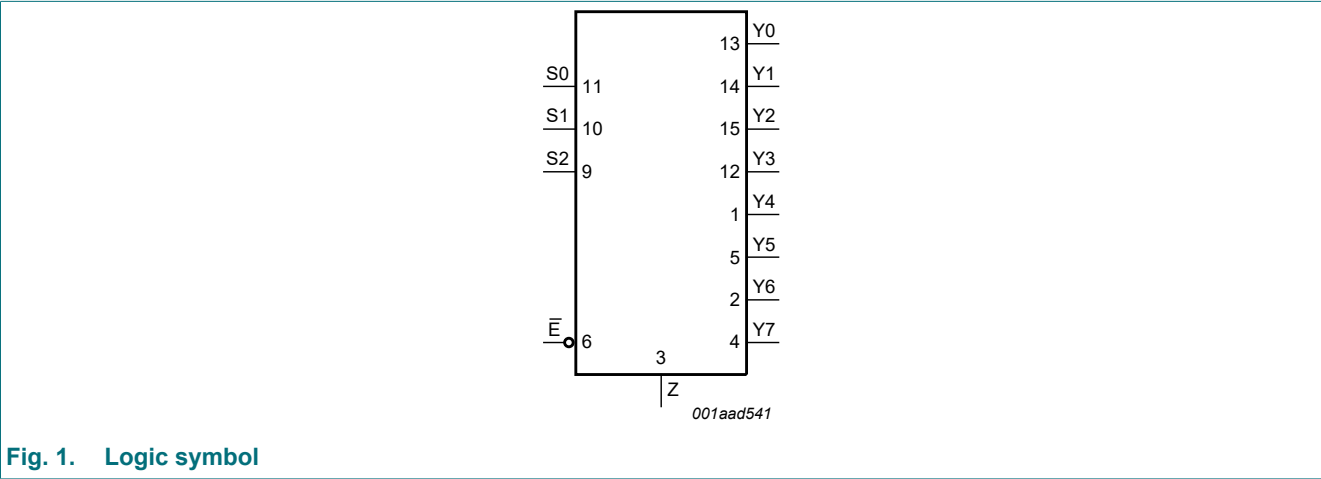


Fig. 1. Logic symbol

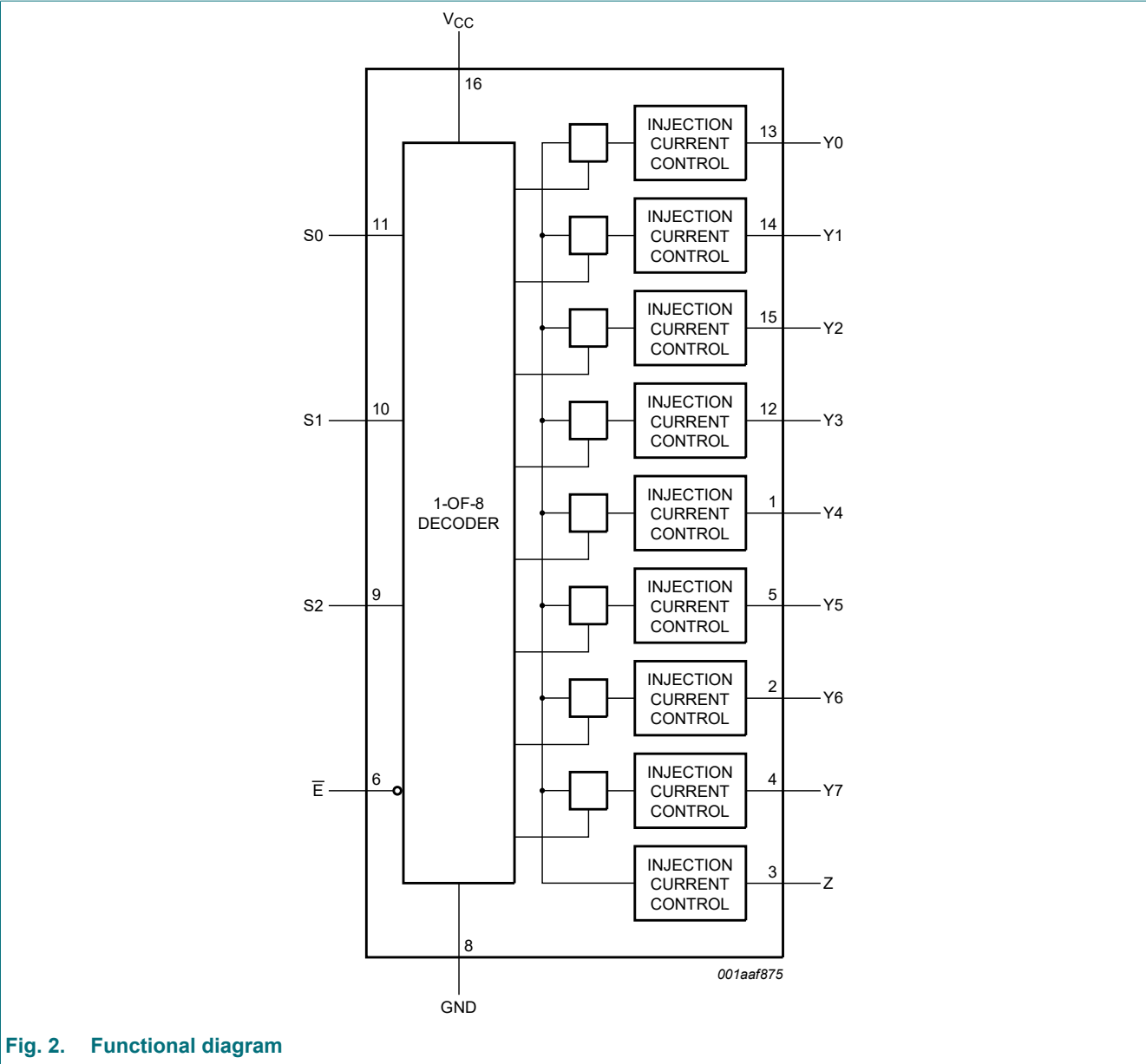


Fig. 2. Functional diagram

7. Pinning information

7.1. Pinning

PW package
SOT403-1 (TSSOP16)

aaa-035182

BQ package
SOT763-1 (DHVQFN16)

aaa-035181

Transparent top view

(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
Y4	1	independent input/output
Y6	2	independent input/output
Z	3	common input/output
Y7	4	independent input/output
Y5	5	independent input/output
E	6	enable input (active LOW); do not leave this pin floating
n.c.	7	not connected
GND	8	ground (0 V)
S2	9	select input; do not leave this pin floating
S1	10	select input; do not leave this pin floating
S0	11	select input; do not leave this pin floating
Y3	12	independent input/output
Y0	13	independent input/output
Y1	14	independent input/output
Y2	15	independent input/output
V _{CC}	16	supply voltage

8. Functional description

8.1. Overview

The NMUX1308-Q100 is a general purpose analog switch with a single pole that can be configured to select between one of eight possible connection paths (SP8T). Each analog connection path is bi-directional, with similar electrical characteristics independent of the direction of signal propagation.

8.2. Key features

Injection current control

Current injection can occur in systems where an analog voltage can experience transient spikes due to signal propagation over long distances with high inductance. Voltage exposure above the supply voltage will source excessive current into an analog input, which is referred to as positive injection. Voltage exposure below the ground voltage will sink excessive current from an analog input, which is referred to as negative injection. Both types of injection current elevate the risk of device damage to an analog input and can introduce a large voltage error to the analog signal itself.

The NMUX1308-Q100 mitigates both risks by integrating an injection current control circuit to divert both positive injection and negative injection through a bypass FET that connects to GND. This implementation minimizes any shift in the supply voltage, therefore minimizing any shift in the device's ON Resistance, and thus minimizes changes in the measured analog voltage. The injection current control circuit is active on all analog pins, independent of whether the channel is selected/unselected.

1.8 V Compatible digital logic thresholds

It is common for modern systems to operate digital signals from lower voltage nodes such as 1.8 V, while operating their analog signals at higher voltage nodes such as 3.3 V or 5.0 V. To remove the requirements for a voltage translation device, the NMUX1308-Q100 digital control pins maintain 1.8 V logic compatible thresholds at higher operating voltages, up to 5.5 V.

I_{off} protection circuitry of digital inputs

The NMUX1308-Q100 implements I_{off} protection circuitry on the digital control pins, isolating those pins from the internal circuits when the supply is unpowered (i.e., $V_{CC} = 0$ V). The ESD protection diodes on the digital input pins do not have a connection path to V_{CC} . If the digital input pins are biased when the V_{CC} pin is unpowered:

1. The high impedance of the digital input pins minimizes input current leakage.
2. The isolation between the digital input pins and the V_{CC} pin ensures no back-powering to the supply rail.

I_{off} protection circuitry of analog inputs/outputs

The NMUX1308-Q100 implements I_{off} protection circuitry on the analog switch pins, isolating those pins from the internal circuits when the supply is unpowered (i.e., $V_{CC} = 0$ V). The ESD protection diodes on the analog switch pins do not have a connection path to V_{CC} . If the analog switch pins are biased when the V_{CC} pin is unpowered:

1. The high impedance of the analog pins minimizes input current leakage.
2. The isolation between the analog pins and the V_{CC} pin ensures no back-powering to the supply rail.

1.5 V to 5.5 V, 8-channel analog switch multiplexer and demultiplexer with injection-current control

3. The high impedance of the analog switch path itself minimizes signal coupling across the switch.

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Channel ON
$\overline{\text{E}}$	S2	S1	S0	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	-

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.0	V
V _I	input voltage	$\overline{\text{E}}$, S0, S1, S2 [1]	-0.5	+6.0	V
V _{SW}	switch voltage	Yn, Z [2]	-0.5	V _{CC} + 0.5	V
I _{SW}	switch current	Yn, Z; V _{SW} > -0.5 V or V _{SW} < V _{CC} + 0.5 V; T _{amb} = -40 °C to +85 °C	-50	+50	mA
		Yn, Z; V _{SW} > -0.5 V or V _{SW} < V _{CC} + 0.5 V; T _{amb} = -40 °C to +125 °C	-25	+25	mA
I _I	input current	$\overline{\text{E}}$, S0, S1, S2	-30	30	mA
I _{GND}	ground current		-100	100	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [3]	-	500	mW
T _j	junction temperature		-	+150	°C

- [1] The minimum and maximum input voltage rating may be exceeded if the input clamping current rating is observed.
[2] The minimum and maximum switch voltage rating may be exceeded if the switch clamping current rating is observed.
[3] For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.5	-	5.5	V
V _I	input voltage	\bar{E} , S0, S1, S2	0	-	5.5	V
V _{SW}	switch voltage	Yn, Z; enable and disable mode	0	-	V _{CC}	V
		Yn, Z; V _{CC} = 0 V	0	-	5.5	V
I _{SW}	switch current	Yn, Z; V _{SW} > GND or V _{SW} < V _{CC} ; T _{amb} = -40 °C to +85 °C	-50	-	50	mA
		Yn, Z; V _{SW} > GND or V _{SW} < V _{CC} ; T _{amb} = -40 °C to +125 °C	-25	-	25	mA
I _{SK}	switch clamping current	Yn, Z; V _{SW} < GND or V _{SW} > V _{CC} [1]	-50	-	50	mA
I _{GND}	ground current		-100	-	100	mA
I _{INJ}	injected current	single off switch	-25	-	50	mA
		all off switches combined	-100	-	100	mA
T _{amb}	ambient temperature		-40	-	+125	°C

[1] If the V_{SW} > V_{CC} or if V_{SW} < GND, the pin will be shunted to GND through an internal FET. The current must be limited within the specified value.

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
Analog switch										
R _{ON}	ON resistance	V _I = V _{CC} to GND; I _{SW} = 0.5 mA; E = V _{IL} ; see Fig. 5								
		V _{CC} = 1.8 V ± 10%	-	450	1151	-	1245	-	1245	Ω
		V _{CC} = 2.5 V ± 10%	-	160	388	-	419	-	436	Ω
		V _{CC} = 3.3 V ± 10%	-	95	231	-	262	-	278	Ω
		V _{CC} = 5 V ± 10%	-	60	146	-	167	-	178	Ω
ΔR _{ON}	ON resistance mismatch between channels	V _I = 0.5V _{CC} ; I _{SW} = 0.5 mA; E = V _{IL}								
		V _{CC} = 1.8 V ± 10%	-	5	91	-	91	-	91	Ω
		V _{CC} = 2.5 V ± 10%	-	4	35	-	39	-	41	Ω
		V _{CC} = 3.3 V ± 10%	-	2	17	-	19	-	19	Ω
		V _{CC} = 5 V ± 10%	-	1	11	-	11	-	12	Ω

1.5 V to 5.5 V, 8-channel analog switch multiplexer and demultiplexer with injection-current control

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{S(OFF)}	OFF-state leakage current	Yn pins; switch off; $\bar{E} = V_{IH}$; $V_I = 0.8V_{CC}$ or $0.2V_{CC}$; $V_O = 0.2V_{CC}$ or $0.8V_{CC}$; see Fig. 3								
		$V_{CC} = 1.8 \text{ V} \pm 10\%$	-	± 1	-	-25	25	-800	800	nA
		$V_{CC} = 2.5 \text{ V} \pm 10\%$	-	± 1	-	-25	25	-800	800	nA
		$V_{CC} = 3.3 \text{ V} \pm 10\%$	-	± 1	-	-25	25	-800	800	nA
		$V_{CC} = 5 \text{ V} \pm 10\%$	-	± 1	-	-25	25	-800	800	nA
		Z pins; switch off; $\bar{E} = V_{IH}$; $V_I = 0.8V_{CC}$ or $0.2V_{CC}$; $V_O = 0.2V_{CC}$ or $0.8V_{CC}$; see Fig. 3								
		$V_{CC} = 1.8 \text{ V} \pm 10\%$	-	± 1	-	-45	45	-800	800	nA
		$V_{CC} = 2.5 \text{ V} \pm 10\%$	-	± 1	-	-45	45	-800	800	nA
		$V_{CC} = 3.3 \text{ V} \pm 10\%$	-	± 1	-	-45	45	-800	800	nA
		$V_{CC} = 5 \text{ V} \pm 10\%$	-	± 1	-	-45	45	-800	800	nA
I _{S(ON)}	ON-state leakage current	Z, Yn pins; switch on; $\bar{E} = V_{IL}$; $V_I = V_O = 0.8V_{CC}$ or $V_I = V_O = 0.2V_{CC}$; see Fig. 4								
		$V_{CC} = 1.8 \text{ V} \pm 10\%$	-	± 1	-	-45	45	-800	800	nA
		$V_{CC} = 2.5 \text{ V} \pm 10\%$	-	± 1	-	-45	45	-800	800	nA
		$V_{CC} = 3.3 \text{ V} \pm 10\%$	-	± 1	-	-45	45	-800	800	nA
		$V_{CC} = 5 \text{ V} \pm 10\%$	-	± 1	-	-45	45	-800	800	nA
C _{SW}	switch capacitance	Yn pins, OFF-state; $V_I = 0.5V_{CC}$; $f = 1 \text{ MHz}$								
		$V_{CC} = 1.8 \text{ V} \pm 10\%$	-	3	10	-	10	-	10	pF
		$V_{CC} = 2.5 \text{ V} \pm 10\%$	-	3	9	-	9	-	9	pF
		$V_{CC} = 3.3 \text{ V} \pm 10\%$	-	3	9	-	9	-	9	pF
		$V_{CC} = 5 \text{ V} \pm 10\%$	-	3	9	-	9	-	9	pF
		Z pin, OFF-state; $V_I = 0.5V_{CC}$; $f = 1 \text{ MHz}$								
		$V_{CC} = 1.8 \text{ V} \pm 10\%$	-	14	23	-	23	-	23	pF
		$V_{CC} = 2.5 \text{ V} \pm 10\%$	-	14	22	-	22	-	22	pF
		$V_{CC} = 3.3 \text{ V} \pm 10\%$	-	14	21	-	22	-	22	pF
		$V_{CC} = 5 \text{ V} \pm 10\%$	-	13	20	-	20	-	20	pF
		Z, Yn pins, ON-state; $V_I = 0.5V_{CC}$; $f = 1 \text{ MHz}$								
		$V_{CC} = 1.8 \text{ V} \pm 10\%$	-	27	31	-	32	-	32	pF
		$V_{CC} = 2.5 \text{ V} \pm 10\%$	-	27	31	-	31	-	31	pF
		$V_{CC} = 3.3 \text{ V} \pm 10\%$	-	27	30	-	31	-	31	pF
		$V_{CC} = 5 \text{ V} \pm 10\%$	-	26	29	-	30	-	30	pF

1.5 V to 5.5 V, 8-channel analog switch multiplexer and demultiplexer with injection-current control

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
Power supply										
I _{CC}	supply current	E, Sn inputs; V _I = GND or V _{CC}								
		V _{CC} = 1.8 V ± 10%	-	-	1	-	1	-	1	µA
		V _{CC} = 2.5 V ± 10%	-	-	1	-	1	-	1	µA
		V _{CC} = 3.3 V ± 10%	-	-	1	-	1	-	1	µA
		V _{CC} = 5 V ± 10%	-	-	1	-	1	-	1	µA

Table 8. Static characteristics

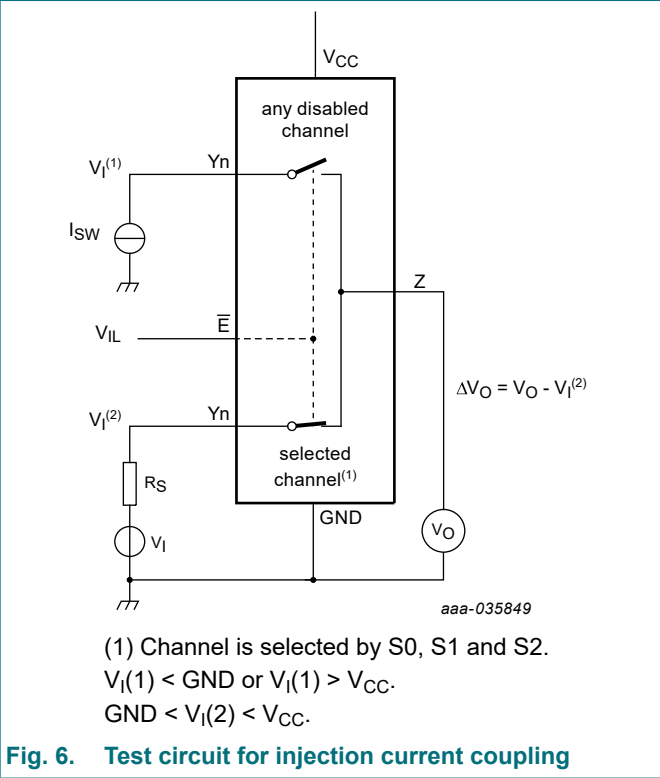
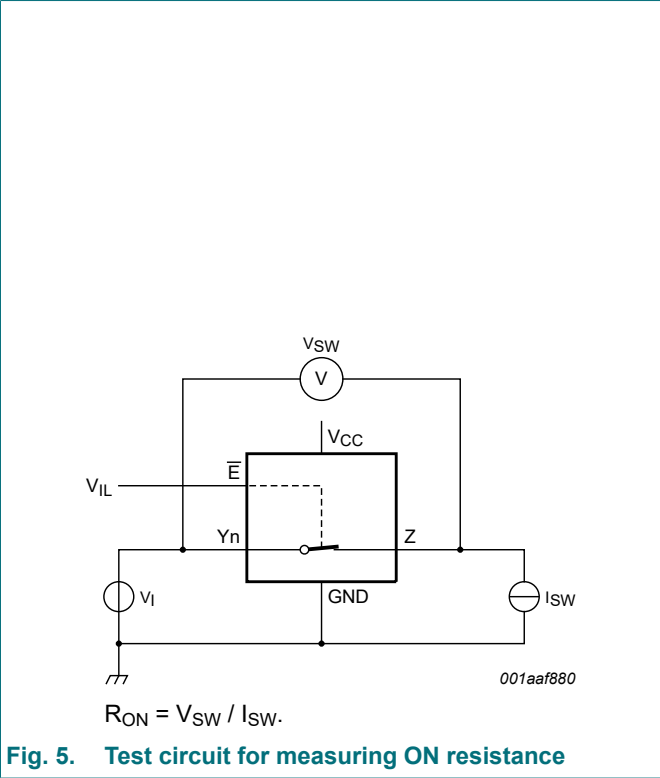
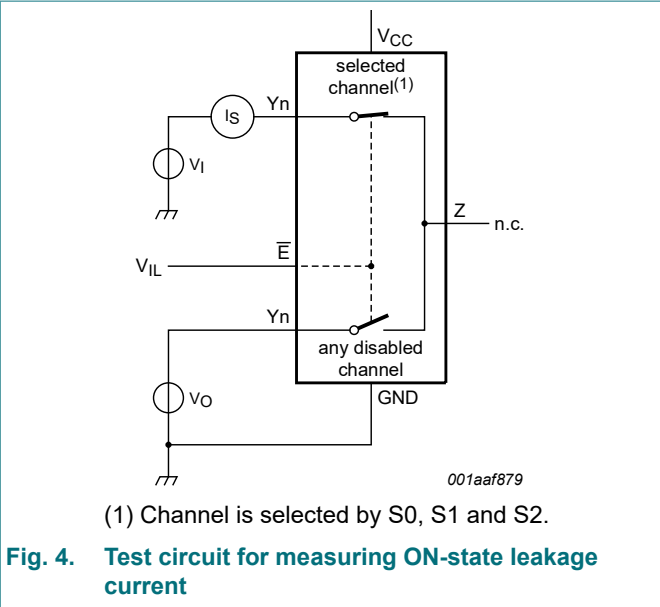
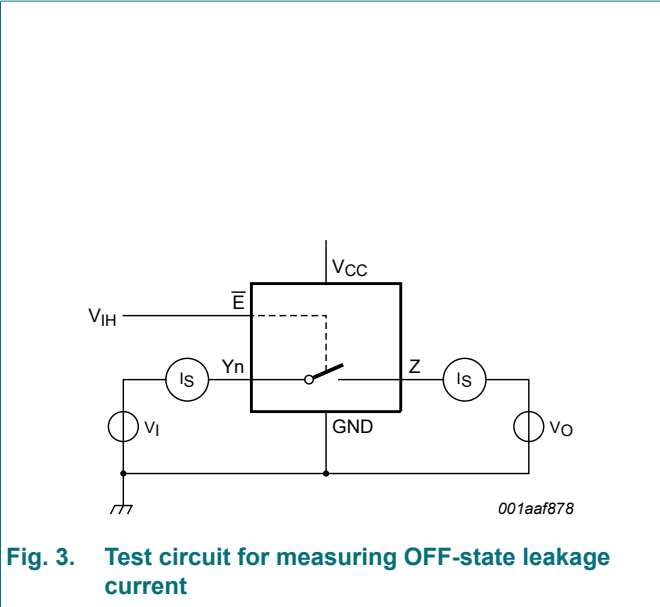
At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 to +125 °C			Unit
			Min	Typ [1]	Max	
Injection current coupling						
ΔV _O	output voltage variation	I _{SW} ≤ 1 mA; R _S ≤ 3.9 kΩ [2] [3]				
		V _{CC} = 1.8 V ± 10%	-	0.1	1	mV
		V _{CC} = 3.3 V ± 10%	-	0.2	1	mV
		V _{CC} = 5 V ± 10%	-	0.4	2	mV
		I _{SW} ≤ 10 mA; R _S ≤ 3.9 kΩ [2] [3]				
		V _{CC} = 1.8 V ± 10%	-	0.1	2	mV
		V _{CC} = 3.3 V ± 10%	-	0.2	2	mV
		V _{CC} = 5 V ± 10%	-	0.4	2	mV
		I _{SW} ≤ 1 mA; R _S ≤ 20 kΩ [2][3]				
		V _{CC} = 1.8 V ± 10%	-	0.1	2	mV
		V _{CC} = 3.3 V ± 10%	-	0.2	2	mV
		V _{CC} = 5 V ± 10%	-	0.4	2	mV
		I _{SW} ≤ 10 mA; R _S ≤ 20 kΩ [2][3]				
		V _{CC} = 1.8 V ± 10%	-	0.1	5	mV
		V _{CC} = 3.3 V ± 10%	-	0.2	5	mV
		V _{CC} = 5 V ± 10%	-	0.4	5	mV
Logic inputs						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.8 V ± 10%	0.99	-	5.5	V
		V _{CC} = 2.5 V ± 10%	1.08	-	5.5	V
		V _{CC} = 3.3 V ± 10%	1.15	-	5.5	V
		V _{CC} = 5 V ± 10%	1.32	-	5.5	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.8 V ± 10%	0	-	0.53	V
		V _{CC} = 2.5 V ± 10%	0	-	0.61	V
		V _{CC} = 3.3 V ± 10%	0	-	0.68	V
		V _{CC} = 5 V ± 10%	0	-	0.79	V
I _{IH}	HIGH-level input current	V _I = 1.8 V or V _{CC}	-	-	1	μA
I _{IL}	LOW-level input current	V _I = 0 V	-1	-	-	μA

1.5 V to 5.5 V, 8-channel analog switch multiplexer and demultiplexer with injection-current control

Symbol	Parameter	Conditions	-40 to +125 °C			Unit
			Min	Typ [1]	Max	
C _I	input capacitance	S0, S1, S2, and \overline{E} pins; V _I = 0 V, 1.8 V, or V _{CC} ; f = 1 MHz	-	1.5	3	pF

- [1] Typical values are measured at T_{amb} = 25 °C.
- [2] ΔV_O here is the maximum variation of output voltage of an enabled analog channel when current is injected into any disabled channel.
- [3] I_{SW} = total current injected into all disabled channels.



12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	Z to Y _n , Y _n to Z; C _L = 50 pF; see Fig. 7 [1]								
		V _{CC} = 1.8 V ± 10%	-	10	22	-	25	-	26	ns
		V _{CC} = 2.5 V ± 10%	-	6	10	-	11	-	12	ns
		V _{CC} = 3.3 V ± 10%	-	3	6	-	7	-	8	ns
		V _{CC} = 5 V ± 10%	-	2	4	-	5	-	5	ns
		V _{CC} = 5 V ± 10%; C _L = 15 pF	-	1	3	-	3	-	3	ns
t _{pd}	transition time between inputs	Sn to Z; R _L = 10 kΩ; C _L = 50 pF; see Fig. 8 [1]								
		V _{CC} = 1.8 V ± 10%	-	54	93	-	93	-	93	ns
		V _{CC} = 2.5 V ± 10%	-	41	67	-	74	-	74	ns
		V _{CC} = 3.3 V ± 10%	-	36	61	-	71	-	71	ns
		V _{CC} = 5.0 V ± 10%	-	33	60	-	70	-	70	ns
		V _{CC} = 5.0 V ± 10%; C _L = 15 pF	-	31	58	-	70	-	70	ns
		Sn to Y _n ; R _L = 10 kΩ; C _L = 50 pF; see Fig. 8 [1]								
		V _{CC} = 1.8 V ± 10%	-	111	359	-	363	-	364	ns
		V _{CC} = 2.5 V ± 10%	-	99	349	-	351	-	351	ns
		V _{CC} = 3.3 V ± 10%	-	96	344	-	344	-	344	ns
		V _{CC} = 5.0 V ± 10%	-	96	335	-	335	-	336	ns
		V _{CC} = 5.0 V ± 10%; C _L = 15 pF	-	39	93	-	94	-	94	ns
t _{en}	enable time	Ē to Z, Ē to Y _n ; R _L = 10 kΩ; C _L = 50 pF; see Fig. 9 [2]								
		V _{CC} = 1.8V ± 10%	-	15	25	-	27	-	29	ns
		V _{CC} = 2.5 V ± 10%	-	12	17	-	18	-	18	ns
		V _{CC} = 3.3 V ± 10%	-	12	17	-	18	-	18	ns
		V _{CC} = 5 V ± 10%	-	12	17	-	18	-	18	ns
		V _{CC} = 5 V ± 10%; C _L = 15 pF	-	11	16	-	17	-	17	ns

1.5 V to 5.5 V, 8-channel analog switch multiplexer and demultiplexer with injection-current control

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{dis}	disable time	\overline{E} to Z, \overline{E} to Y _n ; R _L = 10 kΩ; C _L = 50 pF; S1 = GND; see Fig. 9 [3]								
		V _{CC} = 1.8 V ± 10%	-	22	47	-	48	-	49	ns
		V _{CC} = 2.5 V ± 10%	-	20	37	-	37	-	37	ns
		V _{CC} = 3.3 V ± 10%	-	18	37	-	37	-	37	ns
		V _{CC} = 5 V ± 10%	-	18	31	-	32	-	33	ns
		V _{CC} = 5 V ± 10%; C _L = 15 pF	-	3	5	-	5	-	6	ns
		\overline{E} to Z, \overline{E} to Y _n ; R _L = 10 kΩ; C _L = 50 pF; S1 = V _{CC} ; see Fig. 9 [3]								
		V _{CC} = 1.8 V ± 10%	-	14	72	-	72	-	72	ns
		V _{CC} = 2.5 V ± 10%	-	11	70	-	70	-	71	ns
		V _{CC} = 3.3 V ± 10%	-	10	70	-	70	-	70	ns
		V _{CC} = 5 V ± 10%	-	9	69	-	69	-	70	ns
		V _{CC} = 5 V ± 10%; C _L = 15 pF	-	6	34	-	34	-	35	ns
t _{b-m}	break-before-make time	R _L = 10 kΩ; C _L = 15 pF; Y _n to Z								
		V _{CC} = 1.8 V ± 10%	1	35	-	1	-	1	-	ns
		V _{CC} = 2.5 V ± 10%	1	30	-	1	-	1	-	ns
		V _{CC} = 3.3 V ± 10%	1	30	-	1	-	1	-	ns
		V _{CC} = 5 V ± 10%	1	30	-	1	-	1	-	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_{en} is the same as t_{PZH} and t_{PZL}.
[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

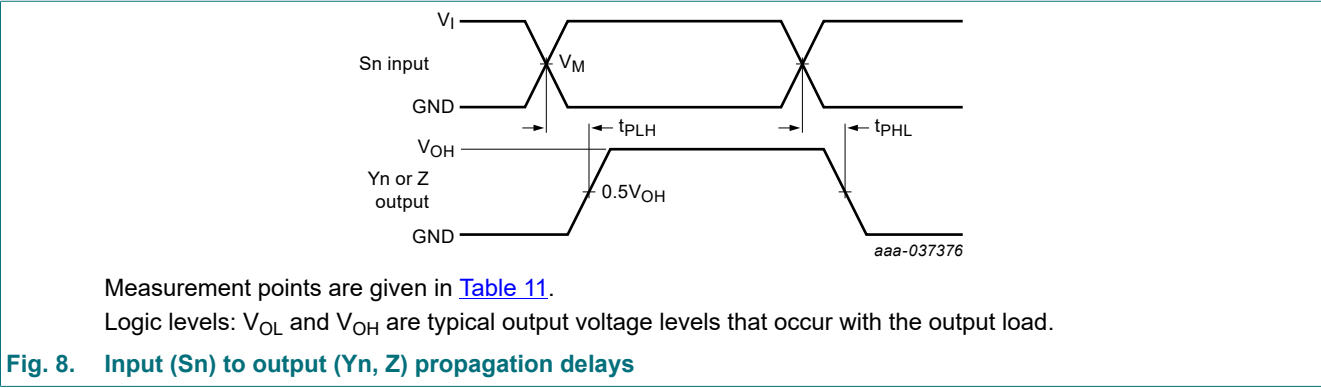
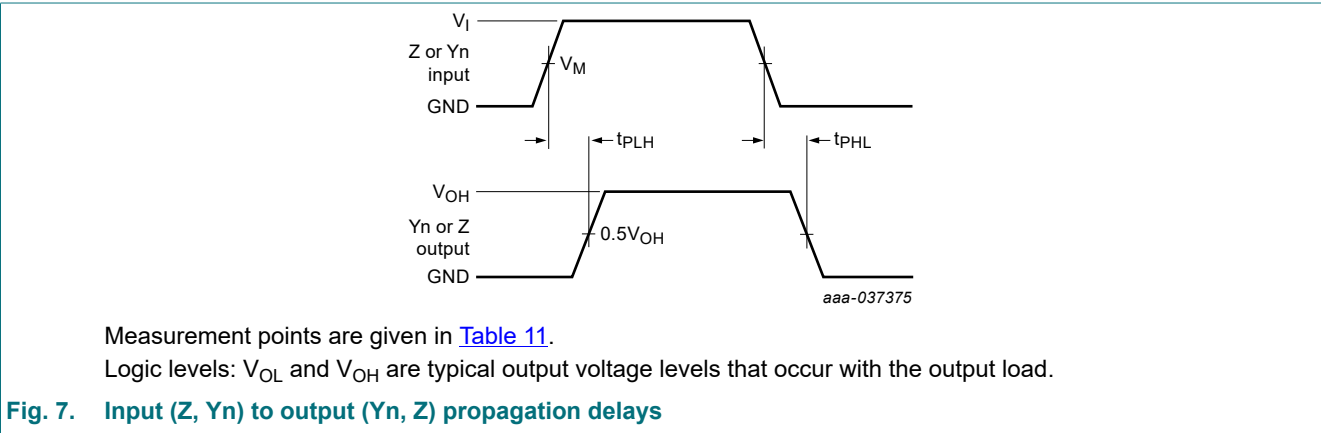
Table 10. Dynamic characteristics

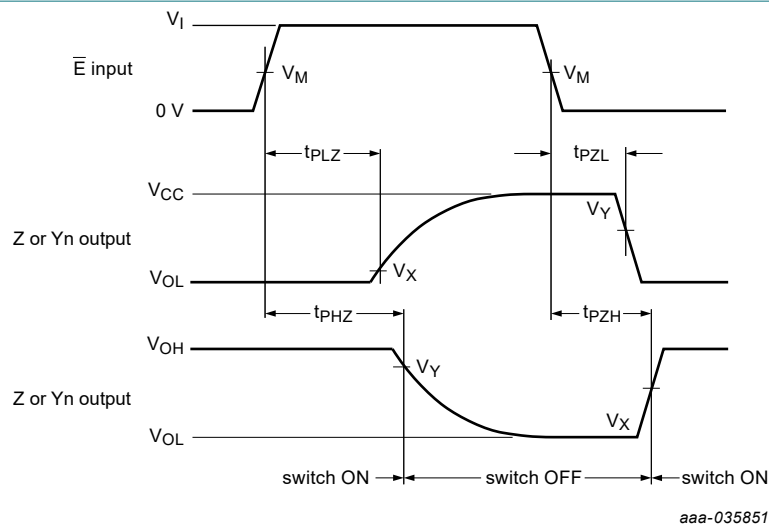
Symbol	Parameter	Conditions	T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	
Q _{inj}	charge injection	V _I = 0.5V _{CC} ; R _S = 0 Ω; C _L = 100 pF				
		V _{CC} = 1.8 V ± 10%	-	1	-	pC
		V _{CC} = 2.5 V ± 10%	-	2	-	pC
		V _{CC} = 3.3 V ± 10%	-	3	-	pC
		V _{CC} = 5 V ± 10%	-	8	-	pC
α _{iso}	isolation (OFF-state)	V _{bias} = 0.5V _{CC} ; V _I = 200 mVpp; R _L = 50 Ω; C _L = 5 pF; f = 100 kHz				
		V _{CC} = 1.8 V ± 10%	-	-125	-	dB
		V _{CC} = 2.5 V ± 10%	-	-125	-	dB
		V _{CC} = 3.3 V ± 10%	-	-125	-	dB
		V _{CC} = 5 V ± 10%	-	-125	-	dB
		V _{bias} = 0.5V _{CC} ; V _I = 200 mVpp; R _L = 50 Ω; C _L = 5 pF; f = 1 MHz				
		V _{CC} = 1.8 V ± 10%	-	-100	-	dB
		V _{CC} = 2.5 V ± 10%	-	-100	-	dB
		V _{CC} = 3.3 V ± 10%	-	-100	-	dB
		V _{CC} = 5 V ± 10%	-	-100	-	dB

1.5 V to 5.5 V, 8-channel analog switch multiplexer and demultiplexer with injection-current control

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	
X _{talk}	crosstalk	V _{bias} = 0.5V _{CC} ; V _I = 200 mVpp; R _L = 50 Ω; C _L = 5 pF; f = 100 kHz				
		V _{CC} = 1.8 V ± 10%	-	-105	-	dB
		V _{CC} = 2.5 V ± 10%	-	-105	-	dB
		V _{CC} = 3.3 V ± 10%	-	-105	-	dB
		V _{CC} = 5 V ± 10%	-	-105	-	dB
		V _{bias} = 0.5V _{CC} ; V _I = 200 mVpp; R _L = 50 Ω; C _L = 5 pF; f = 1 MHz				
		V _{CC} = 1.8 V ± 10%	-	-80	-	dB
		V _{CC} = 2.5 V ± 10%	-	-80	-	dB
		V _{CC} = 3.3 V ± 10%	-	-80	-	dB
		V _{CC} = 5 V ± 10%	-	-80	-	dB
BW	Bandwidth	V _{bias} = 0.5V _{CC} ; V _I = 200 mVpp; R _L = 50 Ω; C _L = 5 pF				
		V _{CC} = 1.8 V ± 10%	-	270	-	MHz
		V _{CC} = 2.5 V ± 10%	-	300	-	MHz
		V _{CC} = 3.3 V ± 10%	-	315	-	MHz
		V _{CC} = 5 V ± 10%	-	325	-	MHz

12.1. Waveforms and test circuit



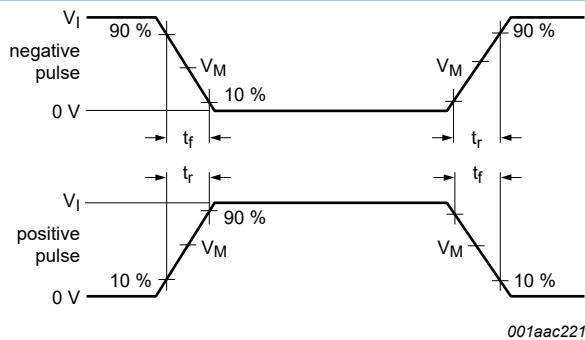


Measurement points are given in [Table 11](#).
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

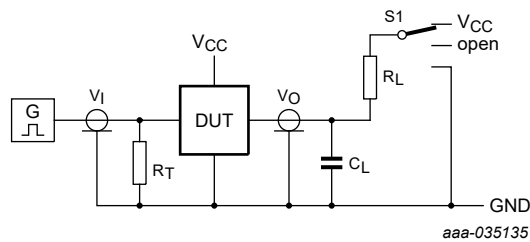
Fig. 9. Enable and disable times

Table 11. Measurement points

Input		Output	
V_M	V_I	V_X	V_Y
$0.5 \times V_{CC}$	V_{CC}	$V_{OL} + 0.1(V_{CC} - V_{OL})$	$0.9 \times V_{OH}$



a. Input pulse definition



b. Test circuit
Test data is given in [Table 12](#).
Definitions for test circuit:
 R_L = load resistance;
 C_L = load capacitance including jig and probe capacitance;
 R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

Fig. 10. Test circuit for measuring switching times

Table 12. Test data

Test	Input			Output		S1 position
	Control E, Sn	Switch Yn (Z)	t _r , t _f	Switch Z (Yn)		
	V _I	V _I		C _L	R _L	
t _{PHL} , t _{PLH}	V _{CC}	V _{CC}	< 5 ns	50 pF	-	open
t _{PHZ} , t _{PZH}	V _{CC}	V _{CC}	< 5 ns	50 pF	10 kΩ	GND
t _{PLZ} , t _{PZL}	V _{CC}	V _{CC}	< 5 ns	50 pF	10 kΩ	V _{CC}

13. Application information

NMUX1308-Q100

The NMUX1308-Q100 is a versatile CMOS bi-directional 8-channel (8:1) analog switch designed for general-purpose use, operating within a voltage range of 1.5 V to 5.5 V. It features 5.5V overvoltage tolerant digital inputs and is compatible with 1.8 V CMOS levels, eliminating the need for voltage translation. The device has also been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1).

Each analog signal pin on the NMUX1308-Q100 incorporates injection current control circuitry. This innovative feature serves to isolate overvoltage spikes on disconnected analog signal pins, preventing them from affecting the connected analog signal path. Two other protective features include Fail-Safe-Logic and Power-off-Protection. These attributes make the NMUX130X family of devices the ideal choice for applications aiming to simplify signal management and reduce system complexity, resulting in a lower component count and a smaller PCB area. This utilization allows users to adopt a design approach centered around modularity, reuse, and scalability.

Typical application schematic

A typical example is provided in [Fig. 11](#). In this instance, various sensor and voltage inputs are sequentially accessed by the input of the SAR ('Successive Approximation Register') ADC. In the example below, the SAR ADC is integrated in the Microcontroller. The operational amplifier serves the purpose of satisfying the SAR ADC recommendation of being driven with a low-impedance source, especially when input sensors or signals have large output impedance. This enhancement improves the performance of the SAR ADC, ensuring fast and accurate conversions while minimizing errors during the sampling process. Additionally, the op-amp eliminates potential error sources, such as ADC input leakage current, that can cause a small drop, resulting in a minor voltage error across the analog multiplexer.

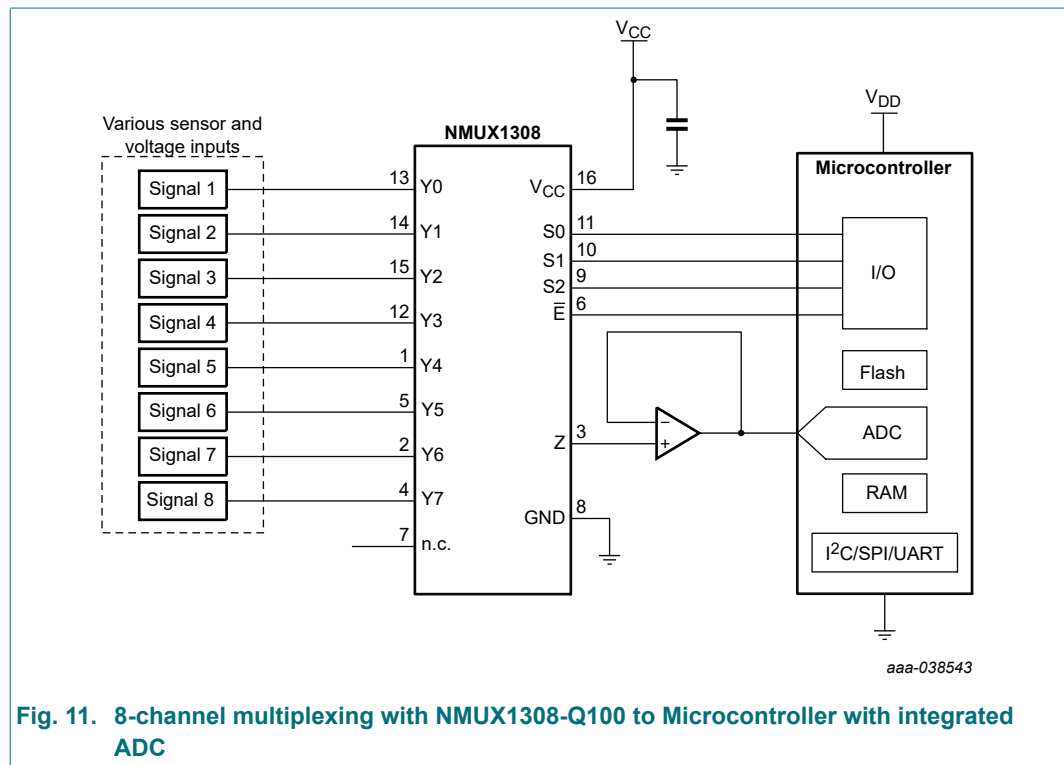


Fig. 11. 8-channel multiplexing with NMUX1308-Q100 to Microcontroller with integrated ADC

1.5 V to 5.5 V, 8-channel analog switch multiplexer and demultiplexer with injection-current control

The benefits of this design type include the capability to route and switch multiple analog signals through a single channel. This is particularly crucial when the number of ADC input channels is limited.

Table 13. Example design parameters with NMUX1308-Q100

Important Design Parameters	Example Value
Supply range (V _{CC})	1.5 V to 5.5 V
Analog input voltage range	0 V to V _{CC} (rail-to-rail)
Control input logic	1.8 V compatible (5.5 V overvoltage tolerant)
I _{SW} independent switch current (maximum)	50 mA
Total analog input continuous current to GND (maximum)	100 mA

Additional example application

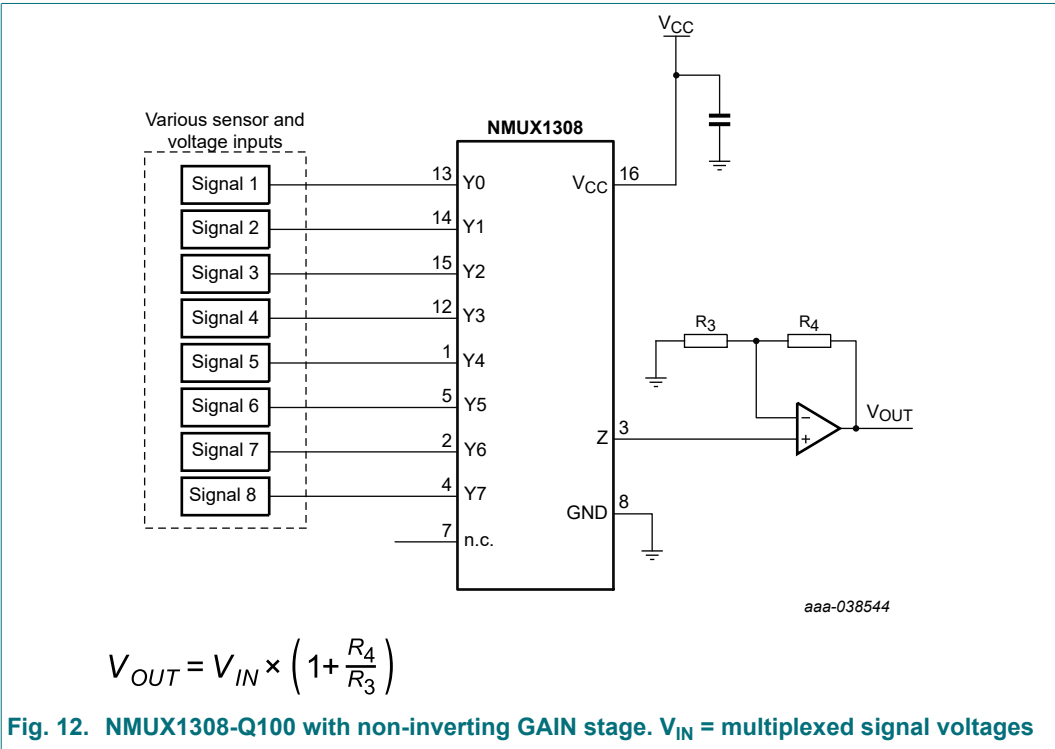
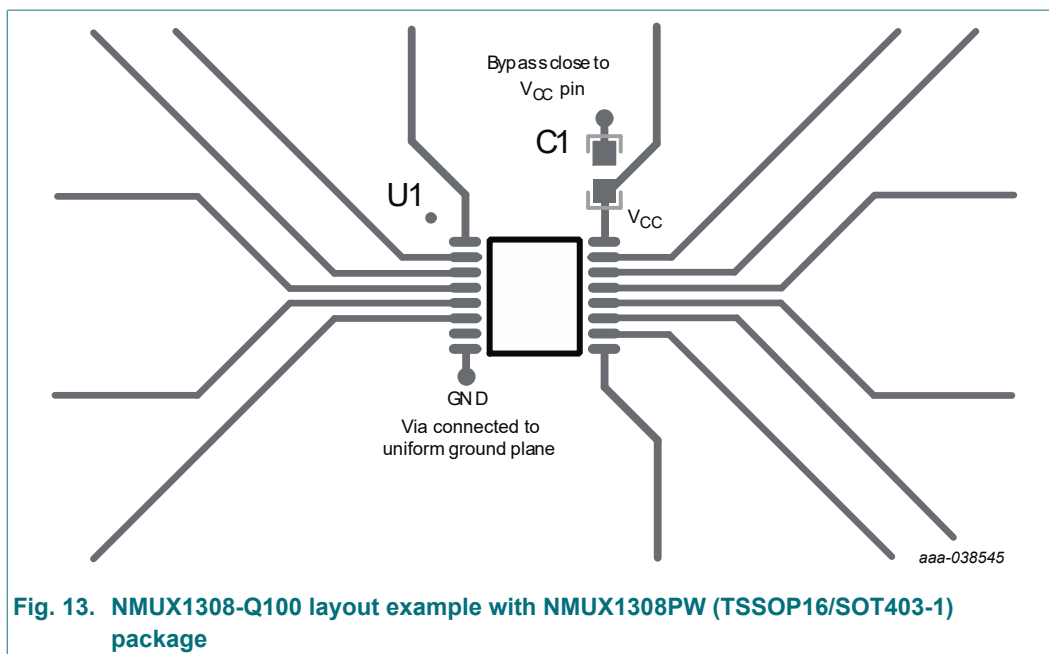


Fig. 12. NMUX1308-Q100 with non-inverting GAIN stage. V_{IN} = multiplexed signal voltages

NMUX1308-Q100 layout example

The image provided below (Fig. 13) offers a glimpse into an example PCB layout with the (PW) package. Bypass capacitors should be positioned near the V_{CC} pin, and the GND pin should be connected to external/internal GND planes. A uniform GND plane helps in reducing noise and minimizing loop inductance, thereby ensuring optimal performance.



Layout recommendations

As with all board designs, proper layout techniques should be employed. Some quick good layout practices and considerations are listed below for quick reference.

- Ceramic capacitors with low ESR should be used to properly decouple or bypass power-supply pins. Ceramic capacitors with high temperature coefficients and low dissipation factors include X5R, X7R and NP0. The recommended minimum value is 0.1 μF .
- For improved noise suppression, additional bypass capacitors can be implemented. It is a common practice to use two different capacitor values to ensure proper filtering of both low-frequency and high-frequency transients. The smaller capacitor, typically in a 0402 package, is placed very near the device pin, while the larger capacitor is positioned farther away.
- To minimize coupling and improve performance all switching nets should travel across a uniform ground plane. Reducing crosstalk can also be achieved by separating traces with a small polygon ground plane.
- Net traces should only have serpentine or 45° bend. Sharper bends, such as 90° should be avoided.

14. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

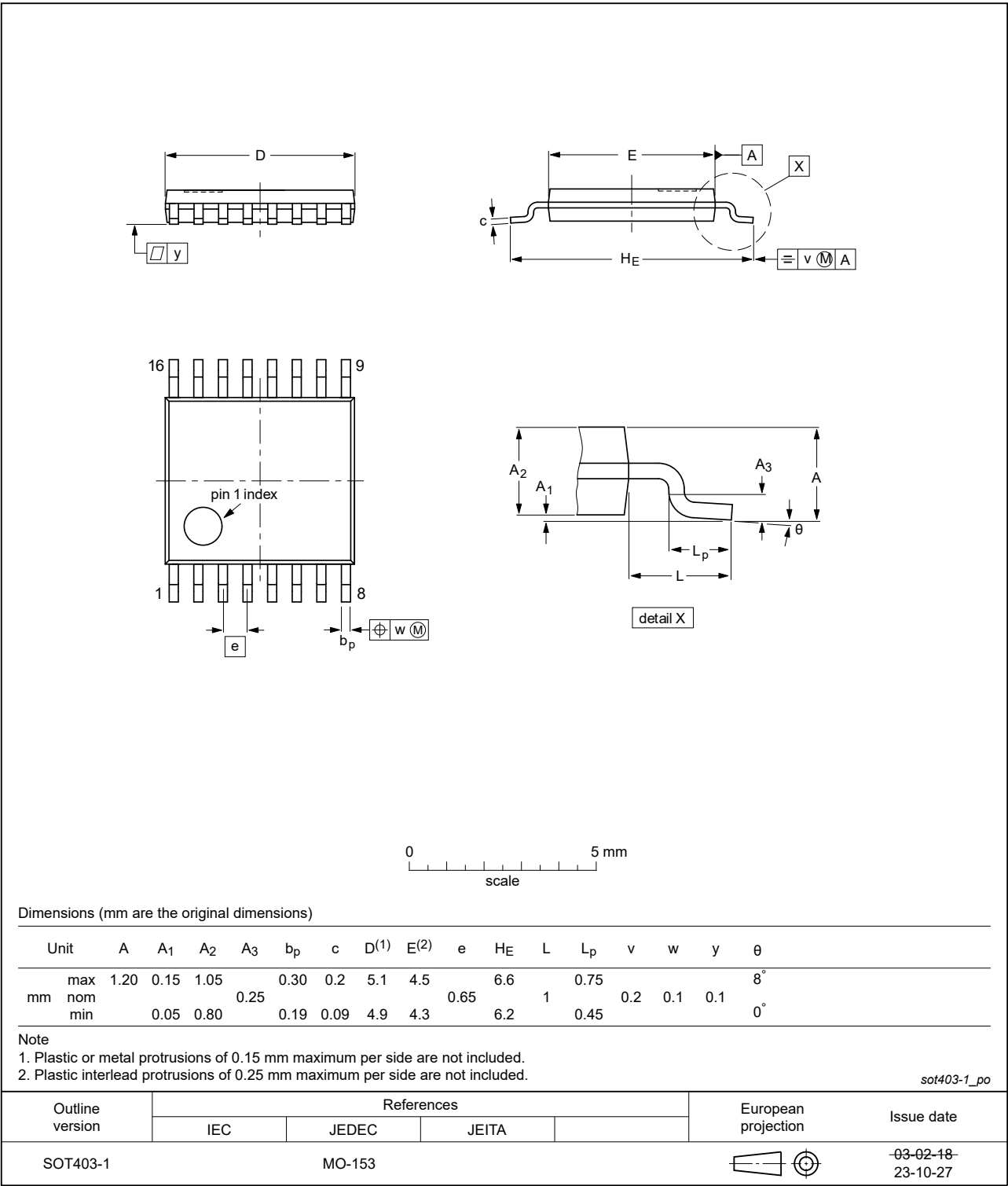


Fig. 14. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

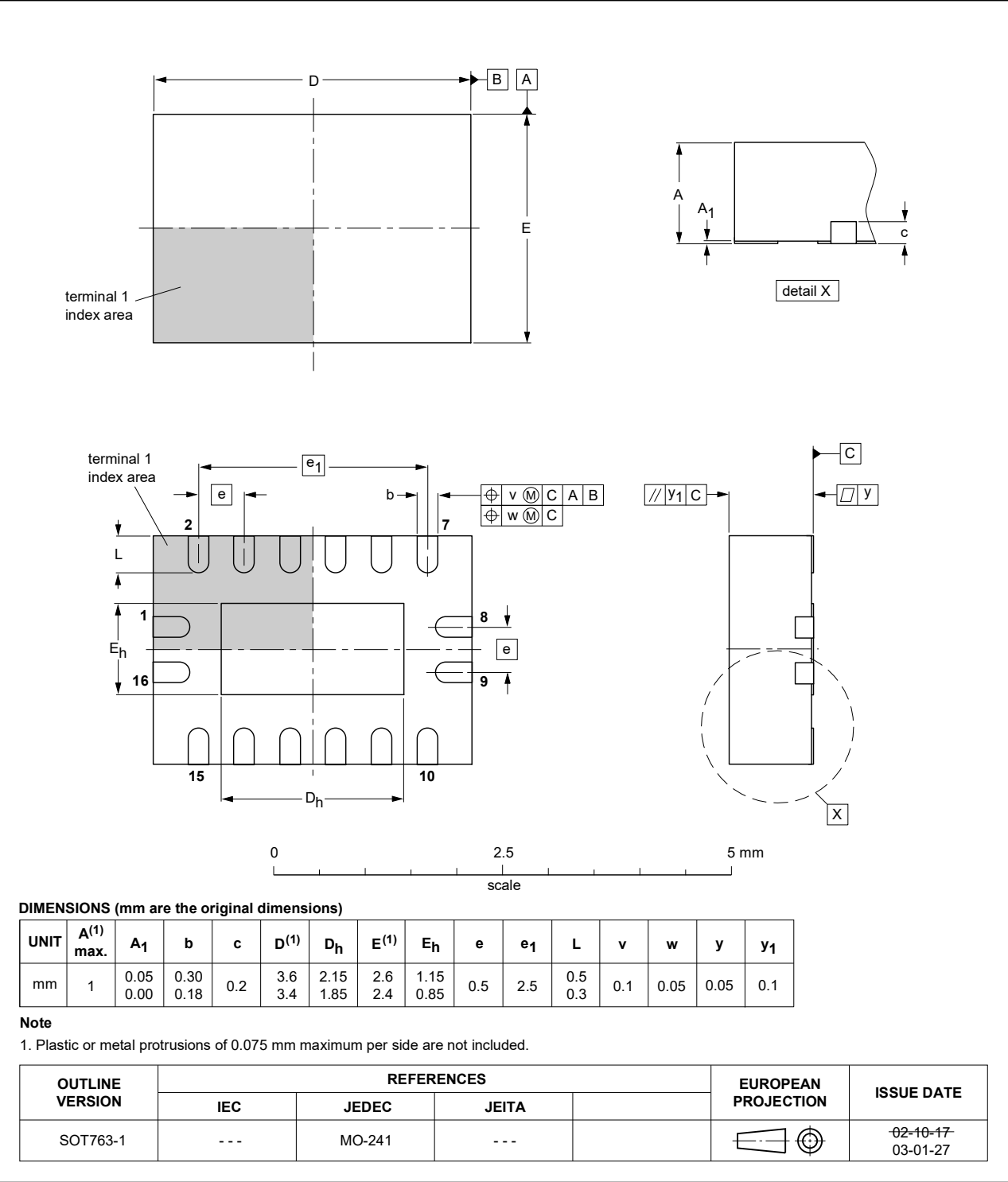


Fig. 15. Package outline SOT763-1 (DHVQFN16)

15. Abbreviations

Table 14. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESDA	ElectroStatic Discharge Association
ESD	ElectroStatic Discharge
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NMUX1308_Q100 v. 1.4	20240823	Product data sheet	-	NMUX1308 v. 1.3
Modification	• Changes to datasheet made for v. 1.3 were added to this table.			
NMUX1308_Q100 v. 1.3	20240725	Product data sheet	-	NMUX1308_Q100 v. 1.2
Modification	• Section 2 : "Automatic Optical Inspection" renamed to "Automated Optical Inspection." • Abbreviation table updated.			
NMUX1308_Q100 v. 1.2	20240416	Product data sheet	-	NMUX1308_Q100 v. 1.1
Modification	• Section 7.1 : Pin configuration drawing of the SOT403-1/TSSOP16 package corrected. (Errata)			
NMUX1308_Q100 v. 1.1	20240221	Product data sheet	-	NMUX1308_Q100 v. 1
Modification	• Fig. 10 : Errata • Section 5 : added			
NMUX1308_Q100 v. 1	20240118	Product data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 2

4. Ordering information.....2

5. Marking.....2

6. Functional diagram.....2

7. Pinning information.....4

7.1. Pinning..... 4

7.2. Pin description.....4

8. Functional description..... 5

8.1. Overview.....5

8.2. Key features..... 5

9. Limiting values..... 6

10. Recommended operating conditions.....7

11. Static characteristics.....7

12. Dynamic characteristics..... 11

12.1. Waveforms and test circuit..... 13

13. Application information..... 16

14. Package outline..... 19

15. Abbreviations.....21

16. Revision history.....21

17. Legal information.....22

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